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| Serial No.: | 10/605,100 | Art Unit: | 2818 |
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IN THE CLAIMS

Claims 1-20 (canceled)

Claim 21 (currently amended): An FET device comprising:

a substrate with a top substrate surface upon which a gate electrode stack is formed;
said gate electrode stack comprising a gate electrode formed over a gate dielectric layer,
said gate dielectric layer being formed on said top substrate surface;
said gate electrode being composed of polysilicon and having a top gate electrode surface
and having gate electrode sidewalls;
sidewall spacer[[s]] material formed on said gate electrode sidewalls aside from said gate
electrode;
a cap layer having outer edges and a top formed on said top gate electrode surface;
notches formed in said outer edges of said cap layer recessed from said gate electrode
sidewalls;
said notches in said outer edges of said cap layer being filled with protective plugs formed
on said top of said gate electrode layer; and
said sidewall spacer[[s]] material reaching along said gate electrode sidewalls to above a
level at which said protective plugs contact said polysilicon of said gate electrode whereby said
sidewall spacer[[s]] material is [[are]] contiguous with and overlapping said protective plugs
covering said sidewalls of said gate electrode.

**Claim 22 (currently amended): The FET device of claim 21 wherein a raised source region and
a raised drain region are formed on said top substrate surface of said substrate aside from said
sidewall spacer[[s]] material.**

**Claim 23 (currently amended): The FET device of claim 21 wherein said protective plugs and
said sidewall ~~spacers are formed of dielectric~~, spacer material comprise a dielectric material.**

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|-------------|------------|-----------|------|
| Serial No.: | 10/605,100 | Art Unit: | 2818 |
|-------------|------------|-----------|------|

Claim 24 (currently amended): The FET device of claim 22 wherein said protective plugs and said sidewall ~~spacers are formed of dielectric~~, spacer material comprise a dielectric material.

Claim 25 (previously presented): The FET device of claim 21 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 26 (previously presented): The FET device of claim 22 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 27 (previously presented): The FET device of claim 23 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 28 (previously presented): The FET device of claim 24 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 29 (currently amended): The FET device of claim 21 wherein ~~[[:]] said gate electrode is composed of polysilicon~~, and said cap layer comprises an ion implanted region formed in said polysilicon of said gate electrode.

| | | | |
|-------------|------------|-----------|------|
| Serial No.: | 10/605,100 | Art Unit: | 2818 |
|-------------|------------|-----------|------|

Claim 30 (currently amended): An FET device comprising:

a substrate with a top substrate surface upon which a gate electrode stack is formed;
 said gate electrode stack comprising a gate electrode formed over a gate dielectric layer,
 said gate dielectric layer being formed on said top substrate surface;
 said gate electrode being composed of polysilicon and having a top surface and having gate
 electrode polysilicon sidewalls;
 sidewall spacer[[s]] material formed on said gate electrode polysilicon sidewalls aside from
 said gate electrode;
 raised source/drain regions formed on said substrate surface aside from said sidewall
 spacer[[s]] material;
 a cap layer having outer edges and a top formed in said top surface of said gate electrode
 comprising an ion implanted region formed in said polysilicon of said gate electrode;
 notches formed in said outer edges of said cap layer recessed from said gate electrode
 sidewalls;
 said notches in said outer edges of said cap layer being filled with said sidewall spacer
material forming protective plugs ~~formed~~ on said top of said gate electrode [[layer]];
 said sidewall spacer[[s]] material being contiguous with and overlapping said protective
 plugs covering said gate electrode polysilicon sidewalls of said gate electrode; and
 said sidewall spacer[[s]] material reaching along said gate electrode sidewalls to above a
 level at which said protective plugs contact said gate electrode polysilicon;
 a raised source region and a raised drain region formed on said top substrate surface of said
 substrate aside from said sidewall spacer[[s]] material.

Claim 31 (previously presented): The FET device of claim 30 wherein said cap layer comprises a thin amorphous silicon layer formed in said gate electrode composed of polysilicon which has been ion implanted with ions selected from the group consisting of germanium and silicon ions.

| | | | |
|-------------|------------|-----------|------|
| Serial No.: | 10/605,100 | Art Unit: | 2818 |
|-------------|------------|-----------|------|

Claim 32 (currently amended): The FET device of claim 30 wherein:

said substrate comprises a Silicon On Insulator (SOI) structure; and

a raised source region and a raised drain region are formed on said top substrate surface of said substrate aside from said sidewall spacer[[s]] material.

Claim 33 (currently amended): The FET device of claim 31 wherein said protective plugs ~~and said sidewall spacers~~ are formed of ~~dielectric~~, said sidewall spacer material which comprises a dielectric.

Claim 34 (currently amended): The FET device of claim 32 wherein said protective plugs ~~and said sidewall spacers~~ are formed of ~~dielectric~~, said sidewall spacer material which comprises a dielectric.

Claim 35 (previously presented): The FET device of claim 30 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 36 (previously presented): The FET device of claim 31 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 37 (previously presented): The FET device of claim 32 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 38 (previously presented): The FET device of claim 33 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

| | | | |
|-------------|------------|-----------|------|
| Serial No.: | 10/605,100 | Art Unit: | 2818 |
|-------------|------------|-----------|------|

Claim 39 (currently amended): The FET device of claim 34 wherein:

~~said gate electrode is composed of polysilicon~~ **said substrate comprises a Silicon On Insulator (SOI) structure; and**

said cap layer comprises an ion implanted region formed in said polysilicon of said gate electrode.

Claim 40 (currently amended): A SOI MOSFET device comprising:

a silicon layer has a surface with a gate electrode stack formed on said surface of said silicon layer;

said gate electrode stack comprises a gate dielectric layer formed on said surface of said silicon layer and a gate electrode with a top formed on said gate dielectric layer;

said gate electrode being composed of gate polysilicon and having polysilicon sidewalls; sidewall spacer[[s]] material formed on said polysilicon sidewalls of said gate electrode;

a cap formed on top of said gate electrode, said cap having a periphery;

a hard mask formed on top of said cap;

said cap being undercut in said periphery of said cap in the form of a notch above said gate electrode and below said hard mask;

said notch being filled with said sidewall spacer material forming dielectric plugs between said gate electrode and said cap to prevent exposure of said gate polysilicon of said gate electrode; and

said sidewall spacer[[s]] material reaching along said sidewalls of said gate electrode and overlapping said plugs; and

raised source/drain regions formed on said surface of said silicon layer aside from said [[s]] sidewall spacer[[s]] material.